RICH VARONE II

Senior Embedded / Firmware Software Engineer
Long Island, NY • work@richardvarone.com
linkedin.com/in/richardvarone • richardvarone.com

SUMMARY

Multidisciplinary senior embedded software engineer with over 14 years of experience designing rugged, safety-critical embedded systems for defense and avionics, with breadth spanning firmware, FPGA/CPLD logic, electrical and mechanical design, and applied AI. Specializes in multi-architecture board support packages (BSPs) and low-level driver development across bare-metal, RTOS (VxWorks, DDC-I Deos, FreeRTOS, and SafeRTOS), Linux, and Windows environments on ARM, PowerPC, Intel/x86, Xilinx, and Altera SoC and SBC platforms. Has led full product developments across software, electrical, mechanical, and test, delivered to the DO-178C (DAL A) standard, and has mentored junior engineers and interns.

EXPERIENCE

Senior Software Engineer II

June 2012 - July 2026

North Atlantic Industries · Bohemia, NY

Leadership & Product Ownership

- Led development of a custom bootloader, delivered as a DO-178C product and deployed across all of the company's ARM products, with features including field firmware updates, multiple boot partitions, startup Built-In Test (SBIT), and FPGA programming, with signature and integrity verification of update images (CRC and hashing) and a hardware root of trust with secure boot on Zynq UltraScale+; worked with the hardware team to enable and integrate Xilinx SEM IP for single-event-upset detection and correction, and DDR-less module builds ran out of the Cortex-A9 L2 cache configured as RAM.
- Led design and development of a modular, multi-function I/O framework spanning multiple hardware and software architectures, architected from the ground up for the DO-178C certification process to maximize artifact reuse; consolidated common code to reduce duplication across products and enable rapid, low-boilerplate development of new I/O modules; roughly 30 module families share one certified core through function-pointer dispatch, so a new module is a table of lifecycle functions rather than a new program.
- Led development of the 75PS4, NAI's 3U cPCI DC/DC converter and a standard catalog product, from a Rev B prototype through qualification to Rev R over 12+ years of improvements, new features, and part obsolescence: owned all of the device firmware in C and a C++/Qt PC application to configure and monitor it, wrote its bare-metal USB CDC device stack from scratch, contributed schematic capture and PCB layout, and directed the electrical and mechanical specialists through routing, qualification, and environmental testing while coordinating with vendors and customers. The product used a multi-MCU, CPU, and FPGA architecture with inter-chip communication across isolation barriers.
- Led development of a 6U VME relay motherboard, built on a Xilinx Zynq-7015 SoC with multiple Altera MAX CPLDs and used as both an internal test tool and a fielded product, handling schematic and layout review, initial board bring-up, FPGA (VHDL) and CPLD logic design, the bootloader, and the RTOS and Linux software.
- Technical lead on many cross-team efforts in a matrixed organization; mentored and onboarded many engineers and interns, reviewed hundreds of candidate resumes and personally interviewed dozens of engineers.
- Built hardware and software that was installed and flown on aircraft, and supported customer flight programs through integration and certification.

Firmware, Drivers & Board Bring-Up

- Delivered firmware and drivers across NAI's C3/C5, G5, and G6 multifunction I/O motherboards, modern SBC line, and CIU/NIU rugged integrated systems: 30+ board and system designs spanning 3U/6U OpenVPX, cPCI, VME, and PCIe, hosting 100+ configurable smart function modules.
- Took new hardware platforms through initial bring-up, integration, troubleshooting, and functional prototype development, bringing up new board designs from power-on and writing low-level bootstrapping code and bootloaders (including U-Boot) and drivers across NXP/Freescale QorIQ PowerPC (T2080/e6500 and P2041/e500mc), NXP Layerscape LX2 (Cortex-A72), Intel Core i7 (11th Gen, Tiger Lake) and Xeon W, and Xilinx Zynq-7000 and Zynq UltraScale+ SoCs, along with a range of NXP/Freescale, STMicroelectronics, Xilinx, and Altera microcontrollers, FPGAs, and CPLDs.
- Created and owned NAIBSP, the company's multi-architecture board support package: a hardware abstraction layer, drivers and a common application API across ARM, PowerPC and Intel, with one source base building as kernel drivers, user drivers, driver clients or the application API. Carried to DO-178C DAL A on multiple projects, shipped on every board and module the company made, used by all engineering staff and by customers directly; held architectural authority and approved every change, and it remains in production. Led BSP, driver and application development across VxWorks (6.x, 7.x), VxWorks Cert Edition, Wind River Helix Virtualization Platform (HVP), DDC-I Deos, NXP Linux, PetaLinux, Wind River Linux, bare-metal, and Windows, including multi-OS bring-up of the 68INT6 SBC. Delivered ARINC 653 time-and-space partitioned avionics builds on VxWorks 653 and DDC-I Deos 653.
- Designed and built the company's Windows KMDF and WDM kernel-mode function drivers for PCI and PCIe devices, working in Windows internals and debugging with WinDbg, and signed production release drivers with Authenticode under an EV code-signing certificate.
- Worked both sides of the PCI and PCIe link: endpoint and device drivers on Linux as kernel drivers and on Windows as KMDF and WDM function drivers for the same hardware, and PCI/PCIe root port development across RTOS, Linux, and bare metal, handling INTx, MSI, and MSI-X interrupt modes, memory-mapped I/O, and DMA.

- Worked with TCP/IP and UDP at the sockets and application-protocol level on Windows and embedded Linux, and integrated the lwIP stack on bare-metal targets against the Ethernet driver and PHY reset and bring-up code written for the same boards.
- Wrote block device and storage drivers and debugged SATA and NVMe problems on NXP Linux, working down through the full Linux SATA stack and into NVMe device firmware, and handled the flash and boot-storage side (NAND and NOR, MTD, wear leveling) behind the bootloader and firmware-update path.
- Debugged kernel-level problems on target with JTAG and hardware debuggers, root-caused kernel oops and panics from dumps and stack traces, and validated kernel and operating-system releases on multi-unit hardware test setups before they shipped.
- Developed the CIU (COSA Integration Unit) low-level software across its Arm Cortex-A53 and Cortex-R5 cores, including the A53 bootloader and bare-metal environment, the R5 BSP, memory-windowing and lock-windowing logic, and a multifunction bare-metal AMP split distributing I/O module functions across two R5 cores, and profiled and optimized boot time and runtime performance. Built bootloaders, bare-metal code, and hardware to low-power requirements, with power optimization at both the firmware and board level.
- Developed firmware and drivers for a broad range of smart I/O and measurement function modules, spanning analog (A/D, D/A), isolated and non-isolated discrete I/O (GPIO, TTL, PWM), relays, synchro/resolver, LVDT/RVDT, RTD/thermocouple, strain-gauge, inertial (accelerometer, gyro, IMU), encoder, variable reluctance, chip detector/fuzz burn, camera/vision, and time-of-flight sensor interfaces.
- Developed communications interfaces and drivers across ARINC 429, MIL-STD-1553, CAN, Ethernet, and serial (RS-422/485) protocols.
- As an intern (2012), built LabVIEW and LabVIEW-RT driver interfaces to the company's I/O hardware and supported customer applications built on them; that work led directly to a full-time offer from the CEO.
- Implemented Built-In Test across startup, background and continuous modes, and authored the Startup BIT library covering eleven board subsystems at host, module and platform scope: memory tested across address bus, data bus and device, flash validating partition and manifest descriptors, and timer and watchdog tests that verify interrupt delivery.

Verification, Test & Process

- Performed schematic and board layout reviews and validated and debugged boards on the bench with JTAG, oscilloscopes, multimeters, spectrum analyzers, and logic analyzers, diagnosing hardware/software integration problems and driving root cause analysis to closure; built automated ATP and DVT test tooling in C#.
- Ran and supported qualification and environmental testing of ruggedized products, personally running some of the EMI, vibration, and environmental testing, including MIL-STD-461 EMI and conducted emissions, temperature, vibration, shock, humidity, and lightning testing, plus environmental stress screening (ESS), under size, weight, and power (SWaP) constraints.
- Managed software configuration at project and program level, including release control, baselines, program-level branching and release sign-off, and drove design changes through the formal engineering change order (ECO) process, supported by acceptance (ATP) and design verification (DVT) testing; practiced Agile development (standups, estimating, retrospectives) with code and design reviews, driving defects to closure.
- Researched thermal management options and recommended solutions; machined housing and heatsink modifications for prototype units; worked with the machinist, 3D scans, and the CAD team on fit and clearance.
- Engaged directly with DERs, auditors and customer certification teams on DO-178C certification, rather than producing evidence for others to present.
- Ran human-in-the-loop testing with operators, sitting with the people using the software and interfaces delivered to them and feeding what was observed back into the design, and drove hardware-in-the-loop and simulator rigs with a person running the scenario.
- Developed and documented software to the DO-178C (DAL A) safety-critical avionics standard, authoring software requirements and requirements-based test cases; helped stand up the company's DO-254 hardware design-assurance process.
- Handled ITAR-controlled and Controlled Unclassified Information (CUI) technical data in accordance with export-control and data-handling requirements.

FIRST Robotics Competition Engineering Mentor *January 2010 - Present*

Bay Shore Union Free School District · Team 271, Bay Shore, NY

- Team lead: administer the program and guide students through requirements, specifications, and the competition build season.
- Architect Team271-Lib, the team's season-agnostic robot framework, on the roboRIO (a Xilinx Zynq-7000 series SoC: Arm Cortex-A9 with FPGA fabric, running NI Linux Real-Time): a state-machine model with per-subsystem exception isolation, deterministic ordered execution, centralized batched CAN signal refresh, and live PID tuning that preserves log-replay determinism.
- Maintain the multi-season robot codebase and lead student software research during the off-season.
- Built a spec-driven, closed-loop AI development system and applied it to the team's competition robot codebase, authoring MCP servers that retrieve and convert match logs off the controller and talk to the live robot over NetworkTables, making PID controller and camera/vision pipeline tuning an AI-in-the-loop activity with safety-gated writes; also build computer-vision pipelines (OpenCV on NVIDIA Jetson) and mentor students in these tools.
- As a student member (2005-2009), served as lead student programmer for three years and team captain for two, writing software for five competition robots under a BAE Systems senior software engineer.

LEADERSHIP & VENTURES

Founder & President, Bay Shore STEAM Corporation *2024 - Present*

501(c)(3) nonprofit · STEAM education · Long Island, NY

- Founded and lead a 501(c)(3) supporting STEAM education and FIRST Robotics Team 271 (The Mechanical Marauders); incorporated and registered the organization across NY, NJ, and MA.
- Architected and deployed the organization's IT as infrastructure-as-code on Microsoft Azure: self-hosted Mattermost and Nextcloud on Ubuntu VMs with managed PostgreSQL/MySQL, VNet/NSG, and Microsoft 365 integration.
- Built the fundraising and grant pipeline: dine-out and retail fundraisers (Blaze, Panera, Savers), a Gene Haas Foundation grant, and corporate sponsors (West Coast Products, Sayville Electric), toward a ~$75,000 annual goal.

Founder, The Crafty Machinist *2023 - Present*

Manufacturing and CNC tooling startup

- Founded a startup making CNC machining and manufacturing tooling affordable and accessible for students, educators, makers, and small businesses, paired with an educational knowledgebase on tool selection, feeds/speeds, and toolpaths.

Founder & Owner, Zip Zap Craft Shack *2020 - 2022*

Laser-engraving & 3D-printing e-commerce maker business

SELECTED PROJECTS

- Project Template: a drop-in scaffold for AI-assisted (Claude Code / Cursor) development with path-scoped AI rules, lint and CI hooks, per-stack overlays (Node, Python, Java, C++, PowerShell, Svelte, Cloudflare, FRC), a citable coding-standard system (mapped to SEI CERT, JPL, Power of Ten), and bundled MCP servers.
- frc-kb: an AI knowledge-base MCP server (TypeScript / Python) using hybrid retrieval (BM25 + embeddings) with a metric-gated eval harness and live sports-data API integrations.
- ERSK: a cross-platform C++23 / Vulkan game-engine framework built to safety-critical software standards (MISRA C:2023, JPL Power of Ten, DO-178C-style lifecycle), applying defense-grade rigor to modern application software.
- BLE Sensor Prototype: Bluetooth Low Energy sensor bring-up on a Nordic nRF52 development kit with Zephyr and the nRF Connect SDK, covering advertising, pairing and bonding, connection handling, and streaming sensor data to a phone.

TECHNICAL SKILLS

Languages: C, C++, C#, Python, JavaScript/TypeScript, Java, VHDL, Verilog, Visual Basic / VB.NET, Assembly, SQL, HTML, XML

AI & Machine Learning: agentic coding tools (Claude Code, Cursor, GitHub Copilot, Antigravity, GLM), spec-driven / closed-loop AI development, LLM APIs and AI agents (RAG, prompt engineering, MCP), computer vision (OpenCV, GStreamer, V4L2, MIPI CSI-2, CMOS image sensors, NVIDIA Jetson, NXP i.MX), on-device model inference (NVIDIA TensorRT on Jetson, OpenCV DNN, vendor NPU/DSP toolchains)

Processors & SoCs: Intel Core i7 (11th Gen, Tiger Lake) and Xeon W; NXP/Freescale QorIQ T2080 (e6500) and P2041 (e500mc) PowerPC; NXP Layerscape LX2 (Cortex-A72); NXP i.MX; Xilinx Zynq-7000 series and Zynq UltraScale+ system-on-chip (SoC) devices; NXP/Freescale Kinetis KL25Z/KL26Z (Arm Cortex-M0+) and STMicroelectronics STM8 microcontrollers; Xilinx, Altera/Intel MAX, and Lattice MachXO2 FPGAs and CPLDs

Boards & System Form Factors: single-board computers (SBCs), multifunction I/O motherboards, smart function modules, rugged integrated systems

Operating Systems: bare-metal, VxWorks (6.x, 7.x), VxWorks Cert Edition, VxWorks 653, Wind River Helix Virtualization Platform (HVP), DDC-I Deos, DDC-I Deos 653, RTEMS, FreeRTOS, SafeRTOS, NXP Linux, PetaLinux, Wind River Linux, Ubuntu, Windows, Zephyr (Nordic nRF Connect SDK)

Virtualization: Proxmox VE (KVM/QEMU and LXC) as a primary development environment, GPU passthrough (VFIO/IOMMU), Wind River Helix Virtualization Platform (embedded hypervisor), Docker

Firmware & Drivers: memory-mapped I/O, interrupt handling, kernel- and user-mode drivers, multi-processor (MCU, CPU, FPGA) architectures, bare-metal USB device stacks (HID, CDC), BSPs, custom and U-Boot bootloaders, multi-core SoC boot flow and AMP core splits; Windows KMDF and WDM kernel-mode drivers, Windows internals, WinDbg, and Authenticode/EV driver signing; PCI/PCIe device drivers on Linux and Windows with INTx, MSI and MSI-X interrupts, plus root port bring-up; block device and storage drivers; NAND/NOR flash, MTD and wear leveling

Secure Boot & Low Power: hardware root of trust and secure boot (Xilinx Zynq UltraScale+), signed firmware update with signature and integrity verification (CRC, hashing), multiple boot partitions, startup Built-In Test (SBIT), low-power firmware and board-level design, power optimization

Interfaces & Buses: cPCI, OpenVPX, VME, PCIe, Ethernet, USB, SPI, I2C, UART, MIPI CSI-2, CAN, RS-422/485, MIL-STD-1553, ARINC 429, SATA, NVMe, Bluetooth Low Energy (BLE)

Networking: TCP/IP and UDP at the sockets and application-protocol level, lwIP stack integration on bare metal, Ethernet driver and PHY reset and bring-up, network protocol development, WireGuard

I/O & Sensor Interfaces: A/D & D/A, discrete I/O (GPIO, TTL, PWM; isolated & non-isolated), relays, synchro/resolver, LVDT/RVDT, RTD/thermocouple, strain gauge, accelerometer/gyro/IMU, encoders, variable reluctance, chip detector/fuzz burn, camera/vision systems, time-of-flight sensors

Software Tools: Visual Studio, VS Code, Eclipse, Xilinx Vivado, Xilinx XSDK, NXP/Freescale Kinetis Design Studio, Intel/Altera Quartus, Wind River Workbench, Aldec Active-HDL, Cadence Allegro PCB, Git, GitLab, Subversion, Visual SourceSafe,

LabVIEW / LabVIEW-RT, Lattice Diamond, DDC-I OpenArbor, Rapita Verification Suite (RVS), PC-Lint, WinDbg, Nordic nRF Connect SDK

Cloud & DevOps: Microsoft Azure (infrastructure-as-code), Docker, Cloudflare Workers, Linux (Ubuntu), CI/CD (GitHub Actions, GitLab)

Compilers: GCC (GNU, including Arm bare-metal toolchains), Clang/LLVM, Wind River Diab, Microsoft Visual C++ (MSVC)

Qualification & Environmental Testing: MIL-STD-461 EMI, conducted emissions, temperature, vibration, shock, humidity, lightning, environmental stress screening (ESS), qualification testing, SWaP, ruggedized production

Processes & Verification: configuration management (project/program level), engineering change order (ECO) process, ATP & DVT test development, Built-In Test (BIT: startup, background, continuous), structural code coverage (MC/DC), worst-case execution time (WCET) analysis, root cause analysis, Agile/Scrum, code and design reviews, unit testing, defect tracking

Hardware & Lab: SoC and SBC board bring-up, schematic review, board layout, JTAG on-target debug, oscilloscopes, multimeters, spectrum analyzers, logic analyzers

Mechanical & Fabrication: CAD (Autodesk Inventor, Onshape, Fusion 360), CAM (Fusion 360), CNC mill and router, manual lathe, 3D printing, 3D scanning, prototype housing and heatsink modification, thermal management research

Standards: DO-178C (DAL A), DO-254 (process stand-up); MIL-STD-704 and MIL-STD-1275

Coding Standards: MISRA C / C++, NASA and JPL C coding standards, Barr Group Embedded C (BARR-C)

EDUCATION

Rochester Institute of Technology · Rochester, NY *2009 - 2011*

Computer science and math coursework. Left early to pursue full-time software engineering work.

LICENSES & CERTIFICATIONS

NYS CTE (Career & Technical Education) teaching certification: requirements complete, certificate pending district appointment

Professional development (North Atlantic Industries): DO-178C and DO-254 safety-critical avionics; Xilinx / AMD (FPGA, Vivado); DDC-I Deos; Wind River (VxWorks, Workbench); PCB layout, routing, and EMI; MATLAB and Simulink.

ACTIVITIES & AWARDS

- Rockwell Automation Innovation in Control Award, FIRST New York City Regional (Javits Center), 2008, for an autonomous control system using multiple sensors for positioning and safety, including the safety and control system for a powerful pneumatic launcher.
- Delphi "Driving Tomorrow's Technology" Award, FIRST Long Island Regional (Hofstra), 2007, for a camera-based control system using inverse kinematics to position a 4-axis arm and track multiple targets.